# **Design and Implementation of basic AND gate**

**Objective:**

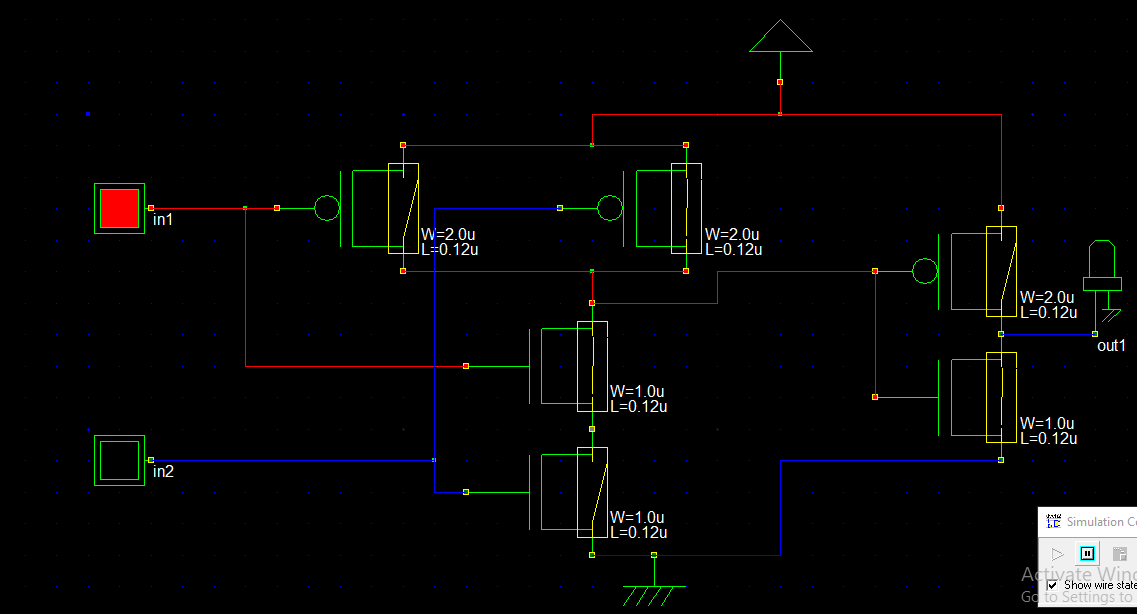
For implementation of And gate, it requires p-mos and n-mos configuration.They may connect with parallel and serial portion. For this basic gate, we can easily solve another gate.

**Theory:** The perform of AND gate find ‘1’ if two input is ‘1’. Otherwise, it will find in the ‘0’.

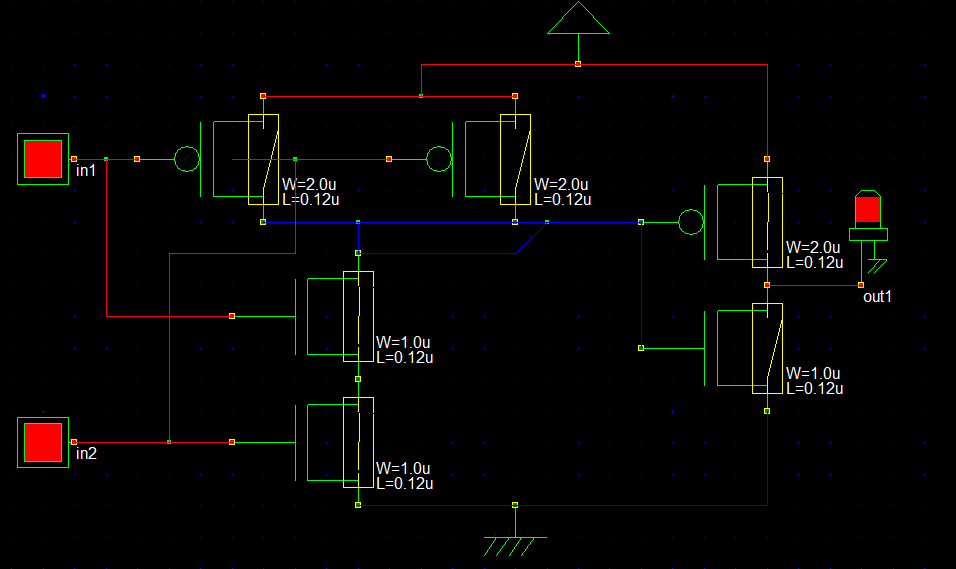
The Table can be written as:

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Circuit Diagram**

If one input 1,other input 0 then output will be as

If two input same as 1, then output will be ON.



**Verilog File**

// DSCH 2.6h

// 9/8/2018 11:59:29 PM

// D:\BOOK\sem 4-1\VLSI\Lab\microwind\andgate.sch

module andgate( in1,in2,out1);

input in1,in2;

output out1;

pmos #(31) pmos(w2,vdd,in1); // 2.0u 0.12u

pmos #(31) pmos(w2,vdd,in2); // 2.0u 0.12u

nmos #(31) nmos(w2,w4,in1); // 1.0u 0.12u

nmos #(10) nmos(w4,vss,in2); // 1.0u 0.12u

pmos #(17) pmos(out1,vdd,w2); // 2.0u 0.12u

nmos #(17) nmos(out1,vss,w2); // 1.0u 0.12u

endmodule

// Simulation parameters in Verilog Format

always

#1000 in1=~in1;

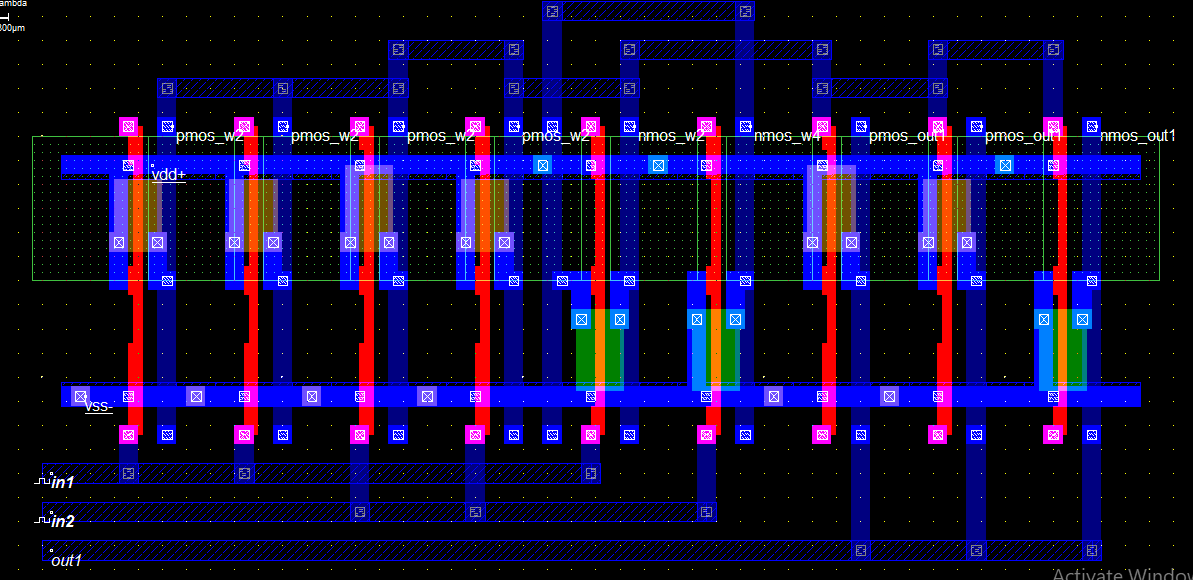
#2000 in2=~in2;

// Simulation parameters

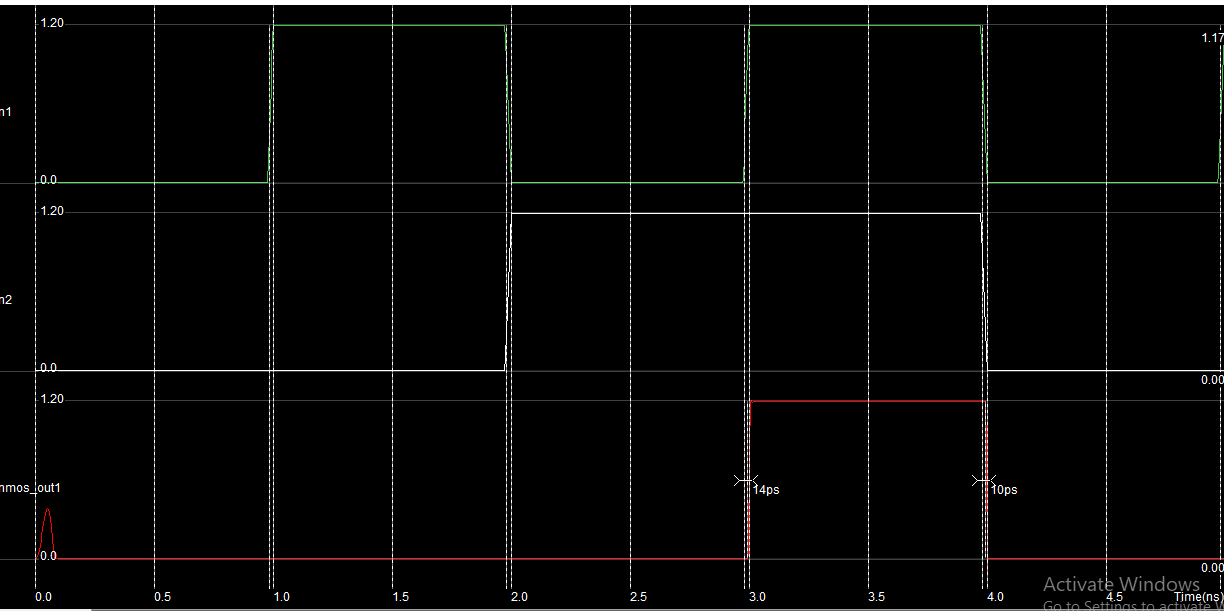
// in1 CLK 10 10

// in2 CLK 20 20

**Layout Diagram**

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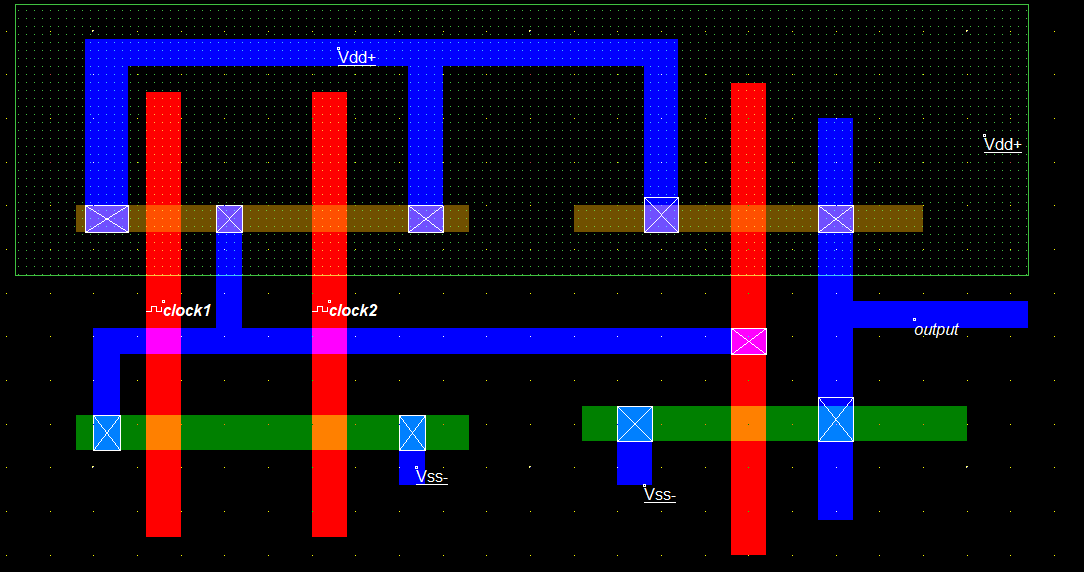
**Timing Diagram**

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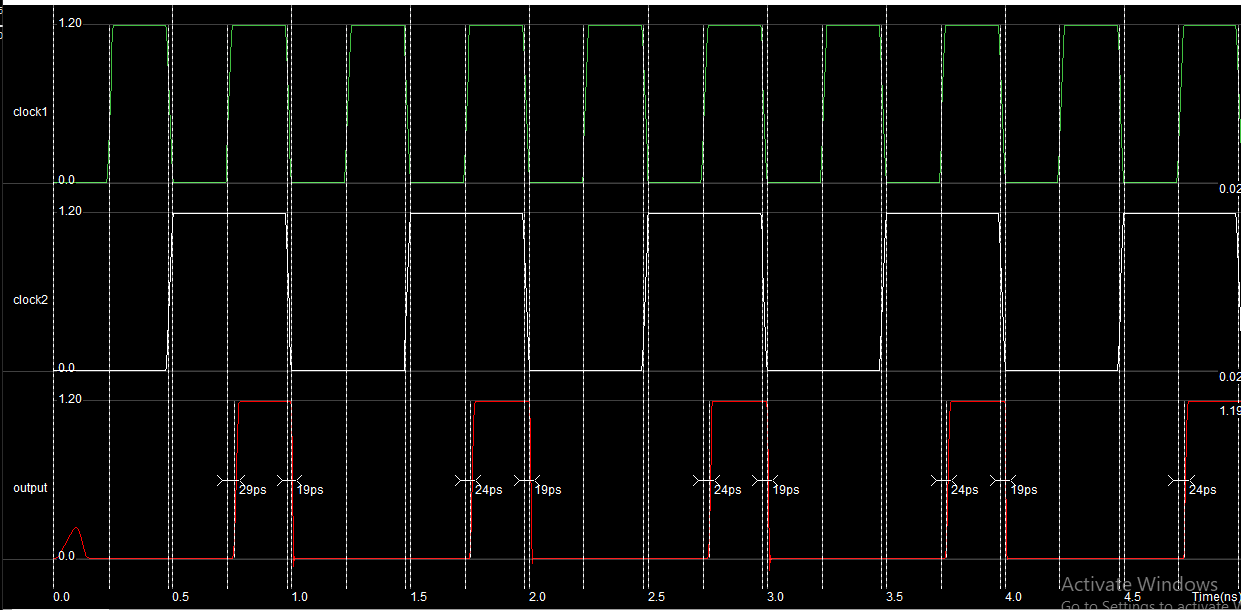
**Discussion**

From this gate, we can easily understand about basic gate of using the DSCH2, and find the stick diagram using the microwind.

**Stick Diagram**

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**Timing Diagram**

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**Design and implementation of basic OR gate**

**Objective:**

For implementation of OR gate, it requires p-mos and n-mos configuration.

They may connect with parallel and serial portion. For this basic gate, we can easily solve another gate.

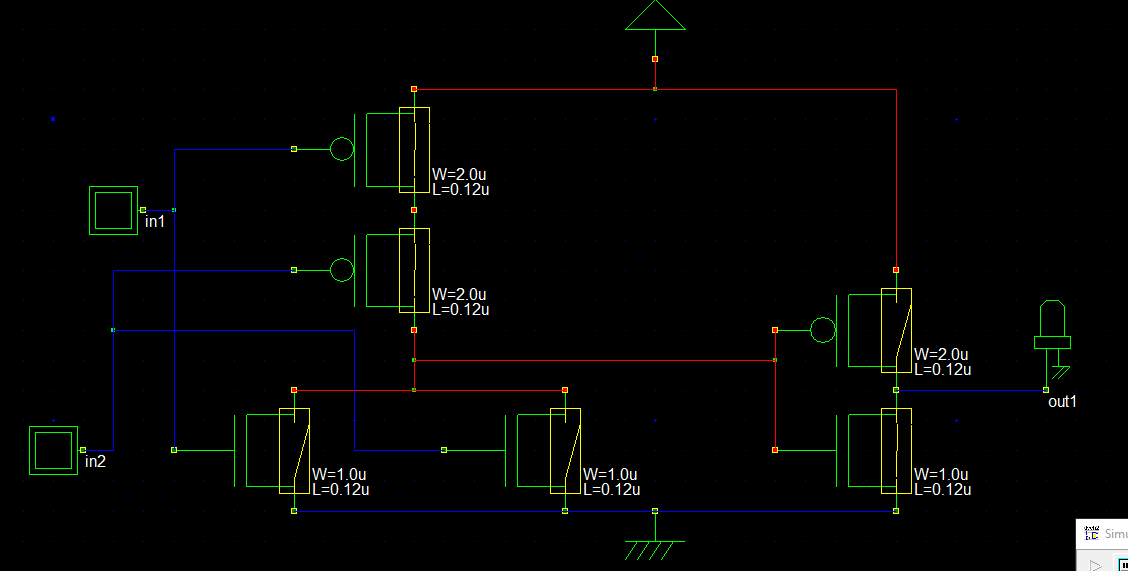
**Theory:** The perform of OR gate find ‘0’ if two input is ‘0’. Otherwise, it will find in the ‘1’.

The Table can be written as:

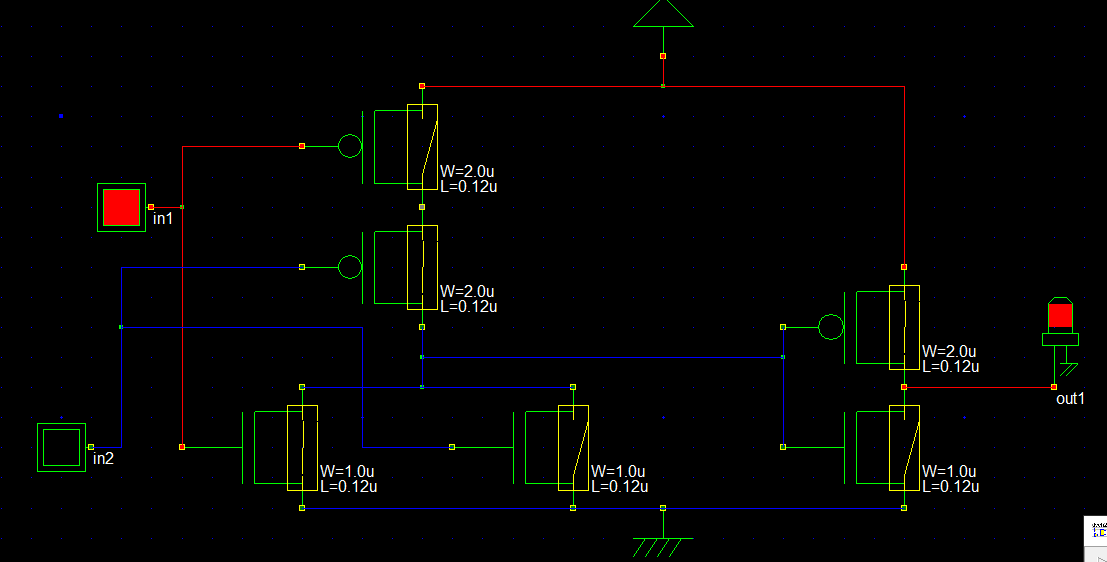
|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**Circuit Diagram**

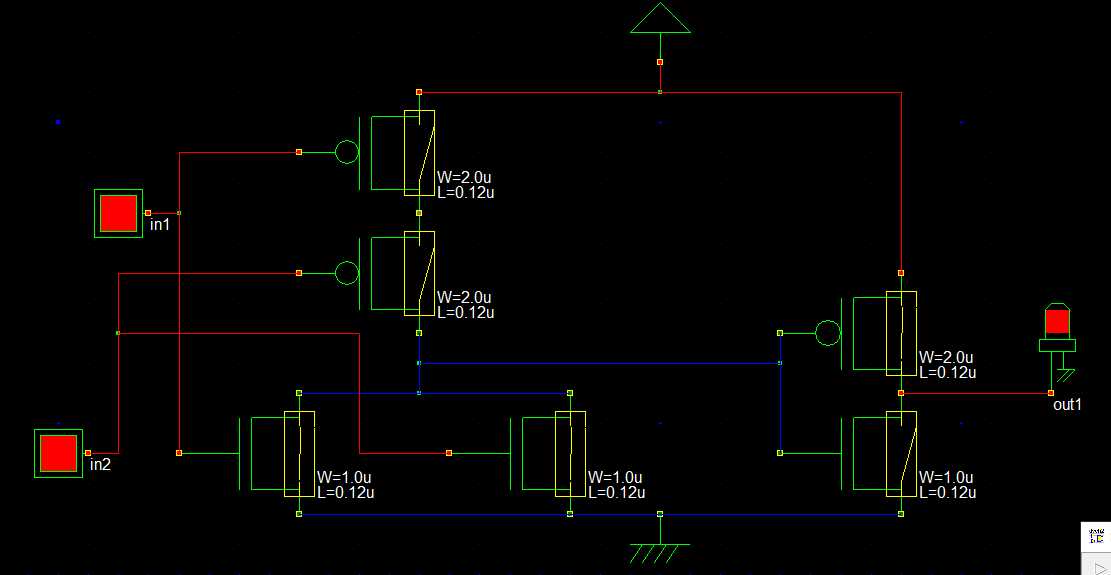
If both input is 0, then output OFF stage.

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If One input is 1,other is 0 then ON stage

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If both input is 1, then also in a ON stage.

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**Verilog File**

// DSCH 2.6h

// 9/9/2018 1:01:38 AM

// D:\tahmina\BOOK\sem 4-1\VLSI\Lab\microwind\orgate.sch

module orgate( in1,in2,out1);

input in1,in2;

output out1;

pmos #(10) pmos(w2,vdd,in1); // 2.0u 0.12u

pmos #(31) pmos(w4,w2,in2); // 2.0u 0.12u

nmos #(31) nmos(w4,vss,in1); // 1.0u 0.12u

nmos #(31) nmos(w4,vss,in2); // 1.0u 0.12u

pmos #(17) pmos(out1,vdd,w4); // 2.0u 0.12u

nmos #(17) nmos(out1,vss,w4); // 1.0u 0.12u

endmodule

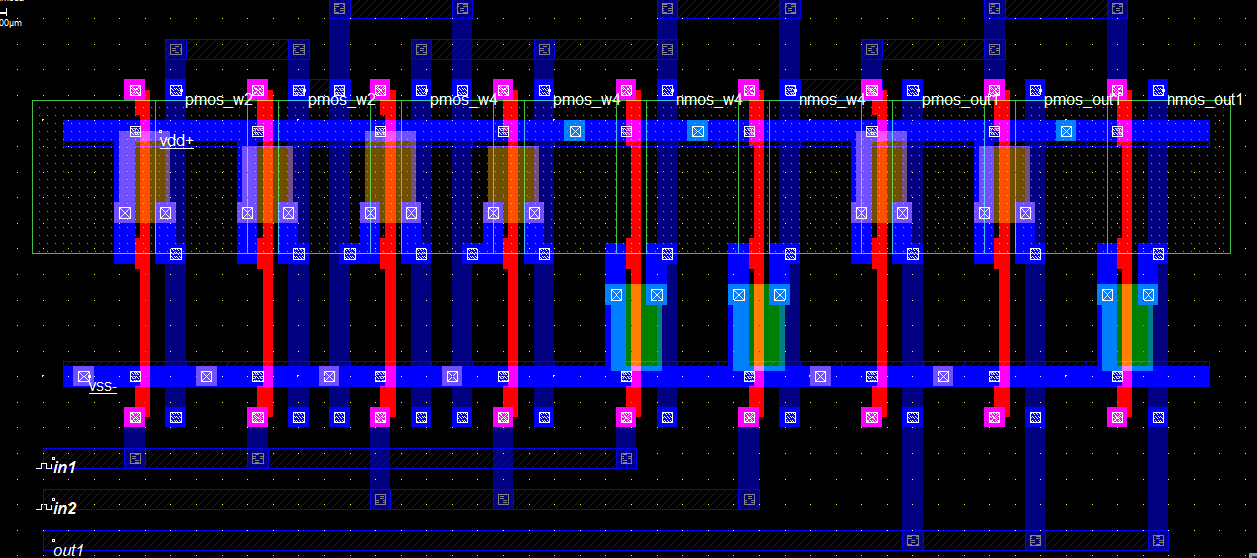
always

#1000 in1=~in1;

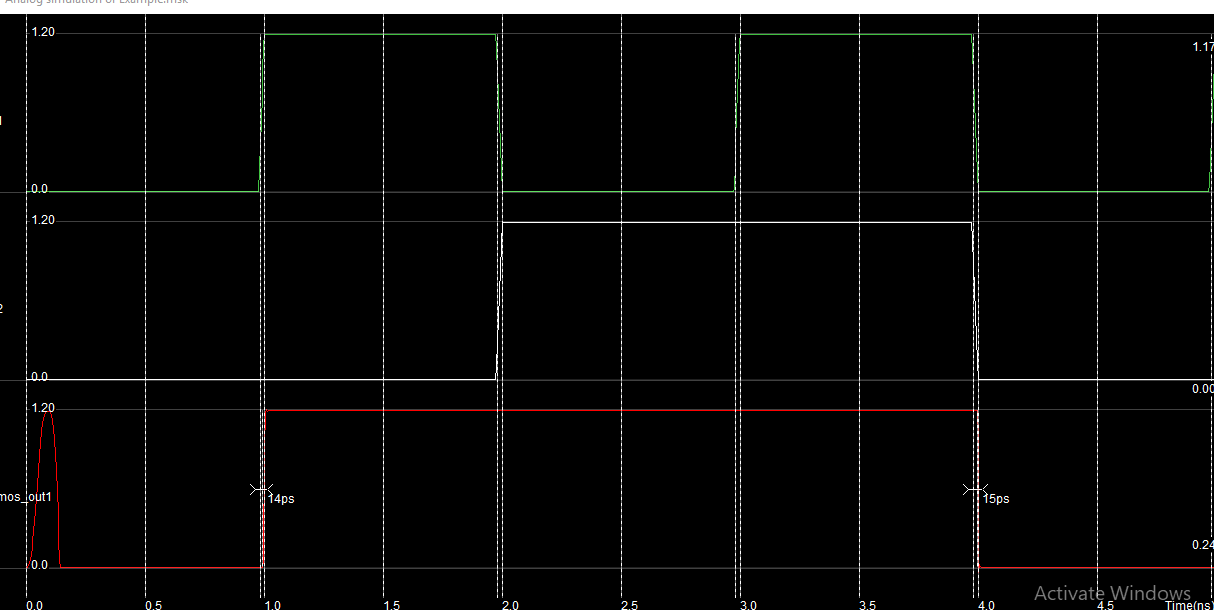
#2000 in2=~in2;

// in1 CLK 10 10

// in2 CLK 20 20

**Layout Diagram**

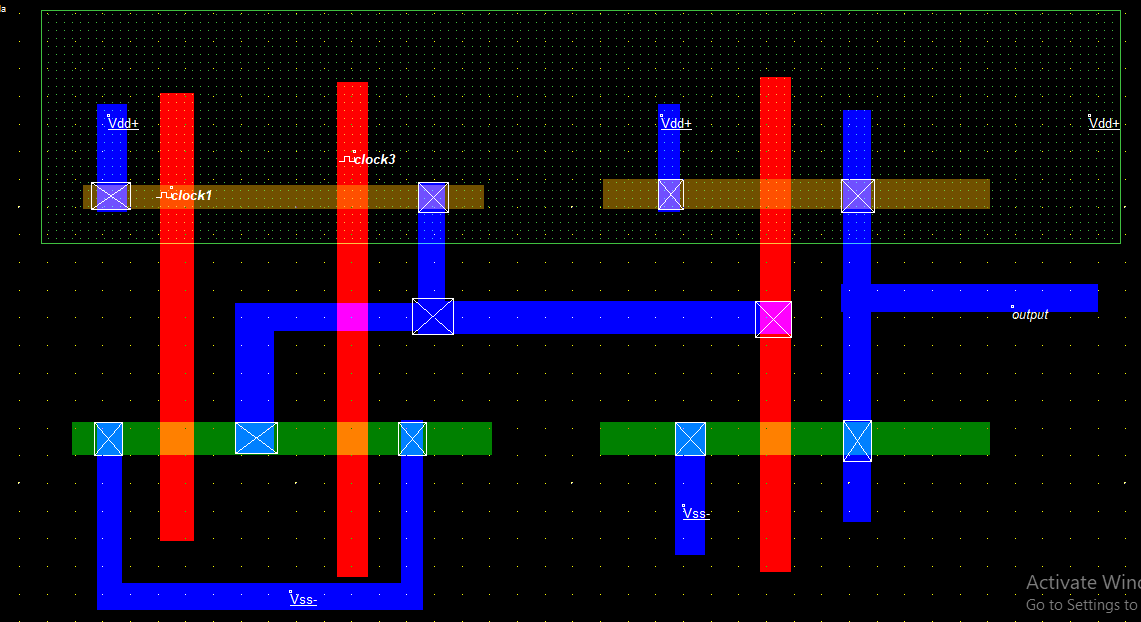
**Timing Diagram**

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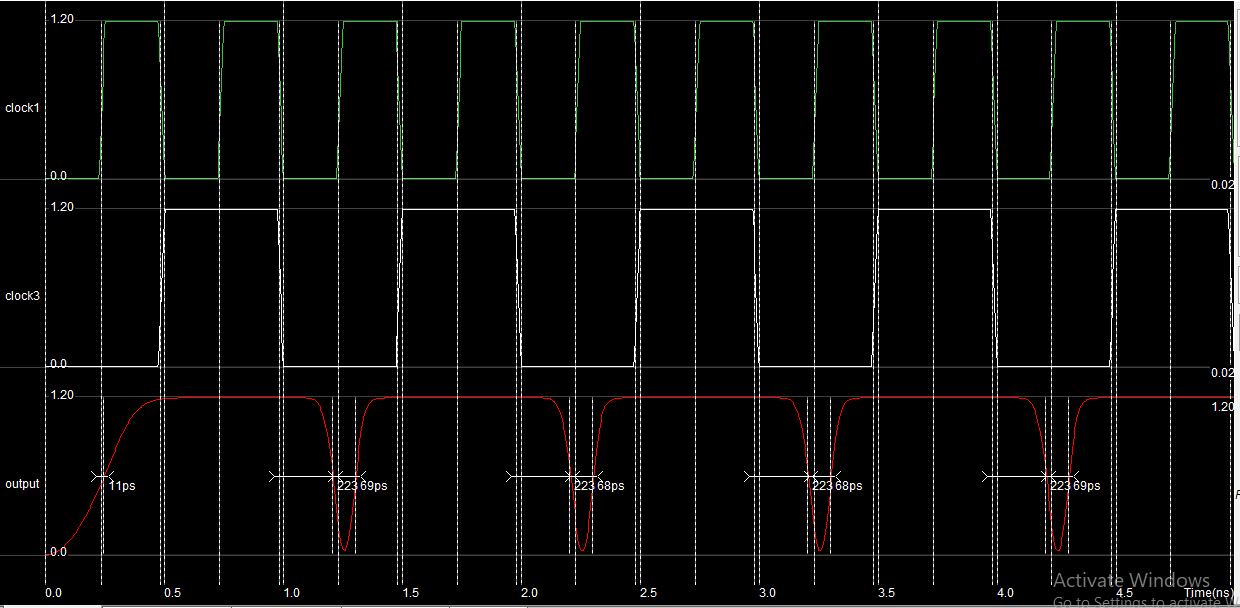
**Discussion**

From this gate, we can easily understand about basic gate of using the DSCH2, and find the stick diagram using the microwind.

**Stick Diagram**

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**OR stick timing diagram**

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**Design and implementation of XOR gate**

**Objective:**

For implementation of XOR gate, it requires p-mos and n-mos configuration.

They may connect with parallel and serial portion. For this basic gate, we can easily solve another gate.

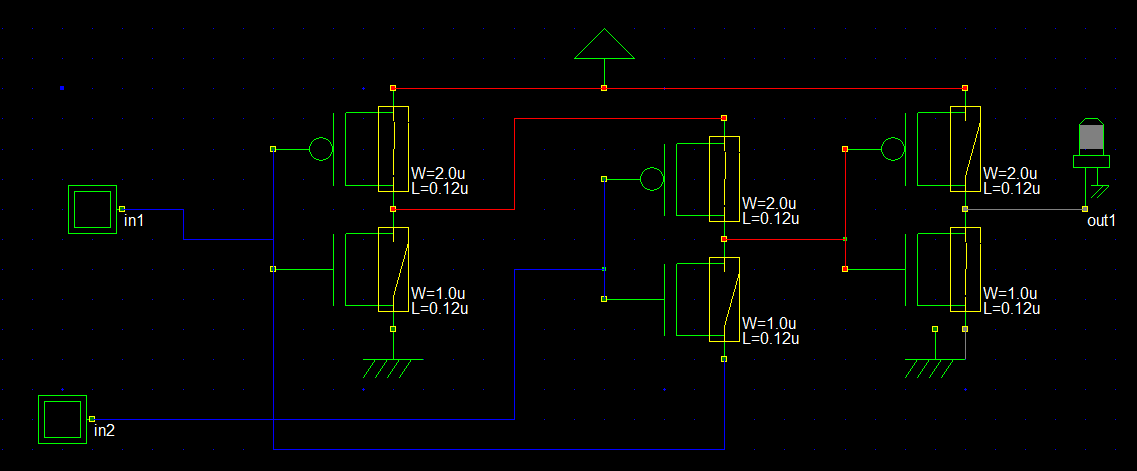
**Theory:** The perform of XOR gate find ‘1’ if one input is ‘1’ and another is ‘0’. Otherwise, it will find in the ‘0’.

The Table can be written as:

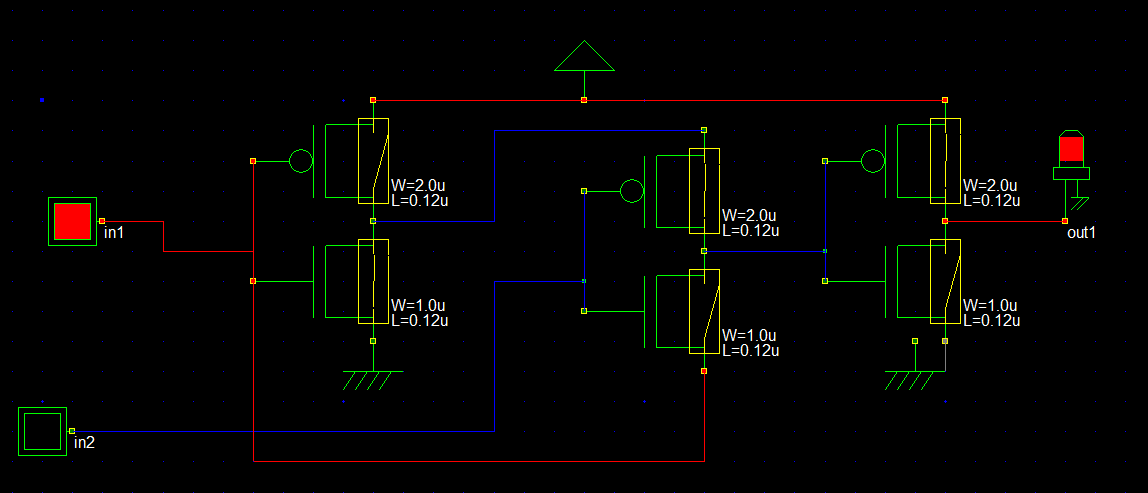
|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Circuit Diagram**

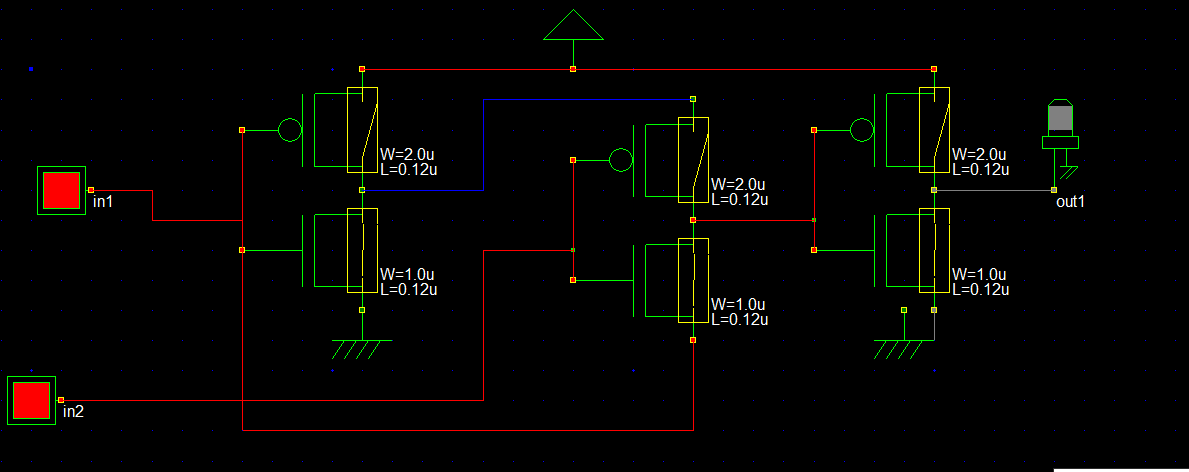
If both input is 0



If one input is 1,other is 0 then output will be ON



If both input is 1, then it will be ON.



**Verilog File**

// DSCH 2.6h

// 9/9/2018 8:38:56 PM

// D:\tahmina\BOOK\sem 4-1\VLSI\Lab\microwind\xor.sch

module xor( in1,in2,out1);

input in1,in2;

output out1;

pmos #(17) pmos(w2,vdd,w1); // 2.0u 0.12u

nmos #(17) nmos(w2,vss,w1); // 1.0u 0.12u

pmos #(24) pmos(w4,w2,in2); // 2.0u 0.12u

nmos #(24) nmos(w4,w1,in2); // 1.0u 0.12u

pmos #(17) pmos(out1,vdd,w4); // 2.0u 0.12u

nmos #(17) nmos(out1,vss,w4); // 1.0u 0.12u

endmodule

always

#1000 in1=~in1;

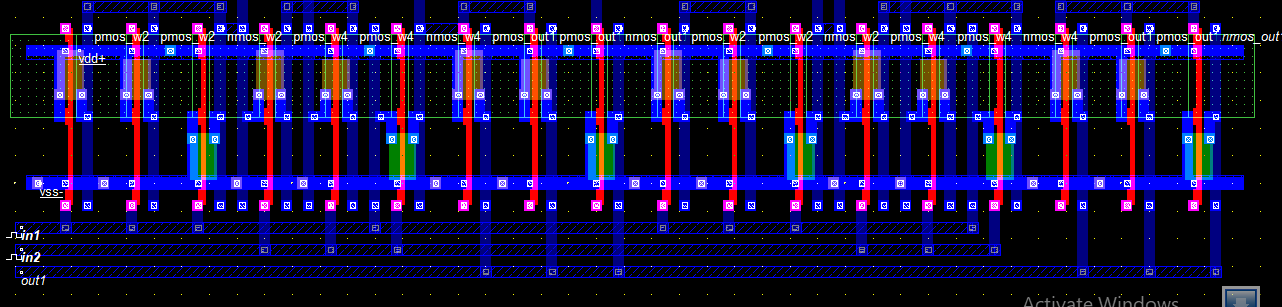
#2000 in2=~in2;

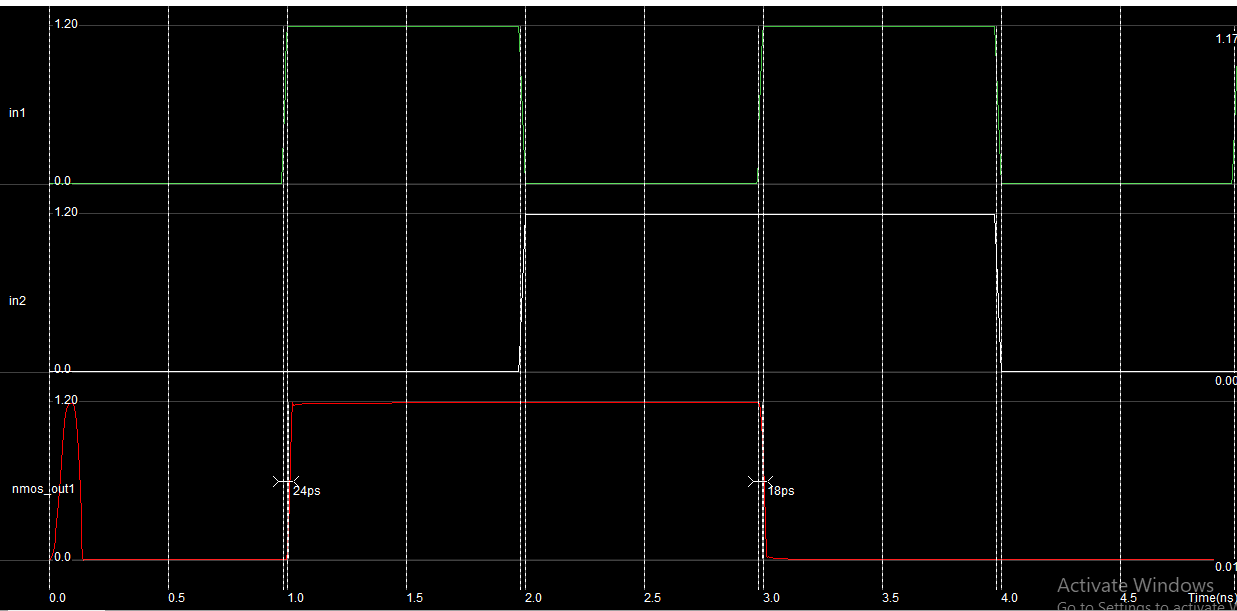
// Simulation parameters

// in1 CLK 10 10

// in2 CLK 20 20

**Layout Diagram**

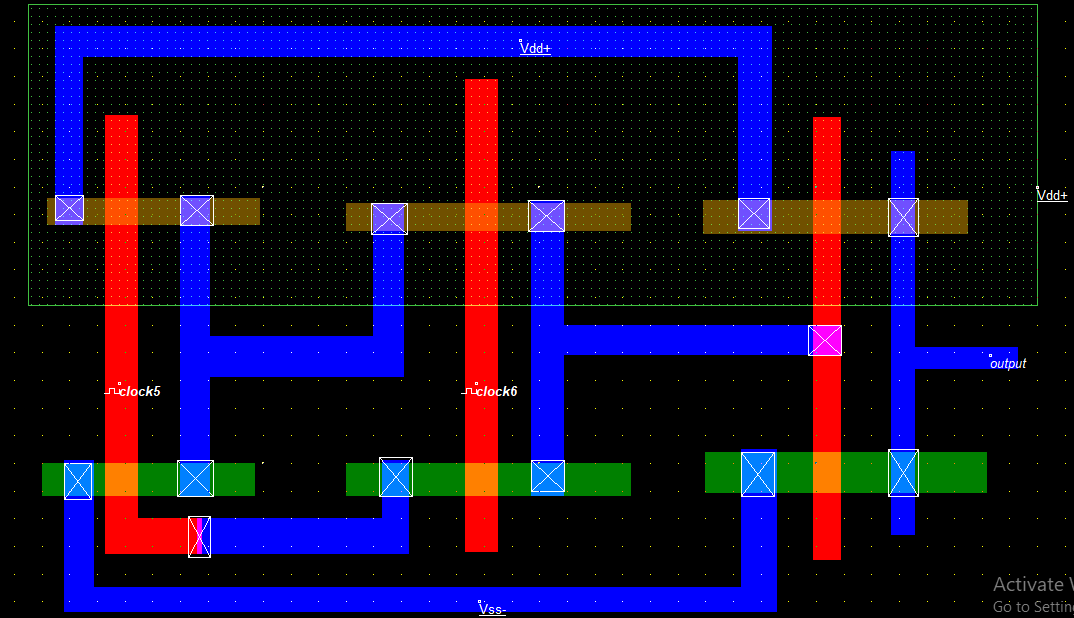
**Timing Diagram**

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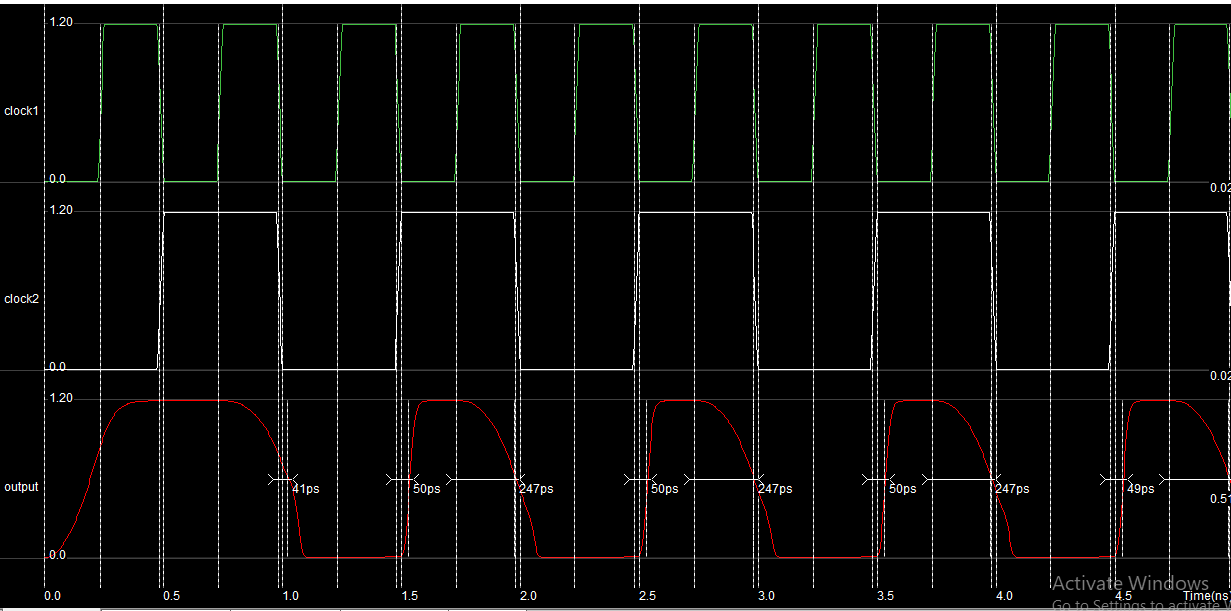
**Discussion**

From this gate, we can easily understand about basic gate of using the DSCH2, and find the stick diagram using the microwind. The gate may be implemented seeing by the source and drain.

**XOR-gate Stick Digram**

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**Stick Timing Diagram**

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